Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A method for reading data from a synchronous memory of the type having data cells arranged in rows and columns and having a single row cache, comprising:

arranging [[the]] said synchronous memory in a symmetrical layout to include a left plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block; a centrally located single row cache; and a right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two;

receiving an initial command and row address data for reading contents of a row of said synchronous memory selected by said row address data;

moving said contents of said row into said single row cache; after said contents of said row have been moved into said single row cache, receiving a "read" command and column address data; and

in response to said "read" command, reading data from said single row cache at a column address specified by said column address data for output by said synchronous memory.

2. (Original) The method of claim 1 wherein said initial command is received substantially concurrently with said row address data.

3. (Original) The method of claim 1 wherein said "read" command and said column address data are received substantially concurrently.

4. (Currently amended) The method of claim 1 further comprising moving said data read from said single row cache to an output of said synchronous memory after a predetermined number of clock cycles after said "read" command.

5. (Currently amended) The method of claim 1 wherein [[said]] moving said data read from said row cache to an output of said synchronous memory after a predetermined number of clock cycles comprises moving said data read from said single row cache to an output of said memory after two clock cycles.

6. (Original) The method of claim 4 wherein said predetermined number of clock cycles is two.

7. (Original) The method of claim 4 wherein said receiving an initial command comprises receiving a "bank activate" command.

8. (Original) The method of claim 1 further comprising performing a first precharging operation prior to receiving said initial command.

9. (Currently amended) The method of claim 1 further comprising initiating a memory operation after said contents of said row have been moved into said single row cache and before said data read from said single row cache has been moved to said output of said synchronous memory.

10. (Original) The method of claim 4 wherein said memory operation is a precharging operation.

11. (Currently amended) The method of claim 9 wherein said synchronous memory is a SDRAM array.

12. (Currently amended) A synchronous memory, comprising:

a symmetrical layout for said synchronous memory including a left plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block; a single row cache centrally located in said symmetrical layout; and a right plurality of N memory portions including a left memory block, a central sense amplifier block, and a right memory block, wherein N is at least equal to two;

means for receiving an initial command substantially concurrently with row

address data and activating for reading a row of said synchronous memory selected by said row address data;

means for moving contents of said row into said single row cache;

means for receiving a "read" command substantially concurrently with column address data after the contents of said row have been moved into said single row cache;

means for reading data from said single row cache at a column address specified by said column address data in response to said "read" command; and

means for moving said data read from said single row cache to an output of said synchronous memory after a predetermined number of clock cycles.

13. (Original) The synchronous memory of claim 12 wherein said means for receiving an initial command comprises means for receiving an initial command substantially concurrently with row address data.

14. (Original) The synchronous memory of claim 12 wherein said means for receiving a "read" command comprises means for receiving a "read" command and column address data substantially concurrently.

15. (Original) The synchronous memory of claim 12 wherein said means for receiving an initial command comprises means for receiving a "bank activate" command.

16. (Original) The synchronous memory of claim 12 further comprising means for performing a first precharging operation prior to receiving said initial command.

17. (Currently amended) The synchronous memory of claim 12 further comprising means for moving said data read from said single row cache to an output of said synchronous memory after a predetermined number of clock cycles after said "read" command.

18. (Currently amended) The synchronous memory of claim 17 wherein said means for moving said data read from said single row cache to an output of said synchronous

memory after a predetermined number of clock cycles comprises means for moving said data read from said single row cache to an output of said memory after two clock cycles.

19. (Original) The synchronous memory of claim 17 wherein said predetermined number of clock cycles is two.

20. (Currently amended) The synchronous memory of claim 17 further comprising means for initiating a memory operation after said contents of said row of said synchronous memory have been moved into said single row cache and before said data read from said single row cache has been moved to said output of said synchronous memory.

21. (Original) The synchronous memory of claim 20 wherein said memory operation is a second precharging operation.

22. (Original) The synchronous memory of claim 12 wherein said memory is a SDRAM array.

23. (Original) An SDRAM adapted to receive a "bank activate" command and a "read" command, comprising:

a central memory region;

a plurality of memory blocks arranged symmetrically in first and second equal-numbered sets on respective opposite sides of said central memory region;

a plurality of primary sense amplifier sets, each set associated with a respective pair of said memory blocks and located adjacent thereto;

a single row cache in said central memory region for selectively caching the contents of each of the plurality of memory blocks on both respective opposite sides of said central memory region;

row decoders for decoding a row address in response to the "bank activate" command and moving data from a decoded row address into a primary sense amplifier set associated with a memory block containing said decoded row address and into said single row cache, prior to application of the "read" command to said SDRAM; and

column decoders for decoding a column address in response to the "read" command and for reading data from said single row cache in accordance with the decoded column address.

24. (Original) The SDRAM of claim 23 further comprising means for moving said data read from said single row cache to an output of said SDRAM a predetermined number of clock cycles after said "read" command.

25. (Original) The SDRAM of claim 23 further comprising means for moving said data read from said single row cache to an output of said SDRAM two clock cycles after said "read" command.

26. (Original) The SDRAM of claim 23 further comprising means for performing a first precharging operation prior to receiving said "bank activate" command.

27. (Original) The SDRAM of claim 23 further comprising means for performing a second precharging operation after said "bank activate" command and prior to said "read" command.